Process Optimization of Rapid Thermal Alloyed Collector Metals Layer in Compound Semiconductor Devices

Stephanie Y. Chang[1]*, Shiban Tiku[1], Lam Luu-Henderson[1], Nercy Ebrahimi[1]

[1]*Skyworks Solutions, Inc., USA*

Email: Stephanie.Chang@skyworksinc.com, +1(805) 871-6801

Abstract

Rapid thermal processing (RTP) is critical within the fabrication flow for alloying an evaporated metal stack (AuGe/Ni/Au) of approximately 200 nm thickness at the eutectic temperature to achieve low contact resistance (R_c). While insufficient alloying results in an incompletely formed collector contact, excessively high temperatures during or downstream from the alloy step results in undesirable diffusion, as depicted in Figure 1.

Therefore, it is essential to take into consideration the downstream effects and tuning of alloy process conditions. As shown in Figure 2's temperature profile, greater stabilization of power and steady intervals of lamp illumination were achieved through the implementation of a series of two moderate ramps and stabilization steps. Furthermore, misalignment or topology of patterned wafers may result in uneven heating. The temperature profile of a batch process' first wafer may also slightly vary due to the quartz chamber's heat capacity and initial temperature after extended idle time. The addition of a preheating step and utilization of graphite susceptors for identical backside conditions facilitates a more consistent run-by-run temperature profile and uniform heating distribution, as shown in Figure 3.

To study the downstream effects on electrical characterization of the collector layer, process control monitor (PCM) structures were measured for R_c after oxidative and thermal processes, as shown in Figures 4 and 5. With a minimal shift in average R_c of 3.24E-3 Ohm-mm between Poly Via 1 (PV1) and end-of-frontside device process, an earlier electrical characterization of collector-related parameters can be achieved and reduce wafer scrap arising from process drifts.

Biography:

Stephanie Chang is a process engineer at Skyworks Solutions, Inc.'s Advance Process Technology Group, specializing in thin films and photo processes. She graduated from UC Berkeley and previously worked at Lawrence Berkeley National Laboratory's Molecular Foundry where she researched liquid cell TEM, MEMS/NEMS, and metamaterials.

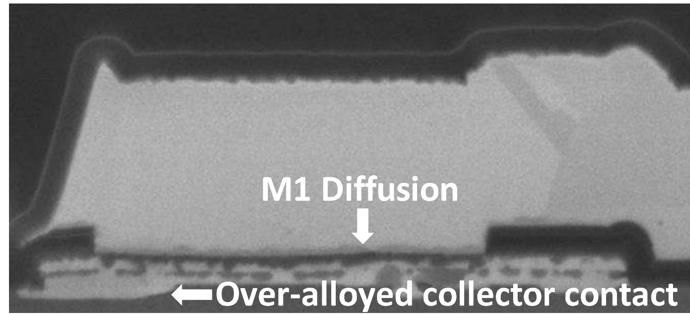

Figure 1. High temperature processes downstream from Metal 1 (M1) deposition resulted in an over-alloyed collector contact metal stack and diffusion into the M1 layer.

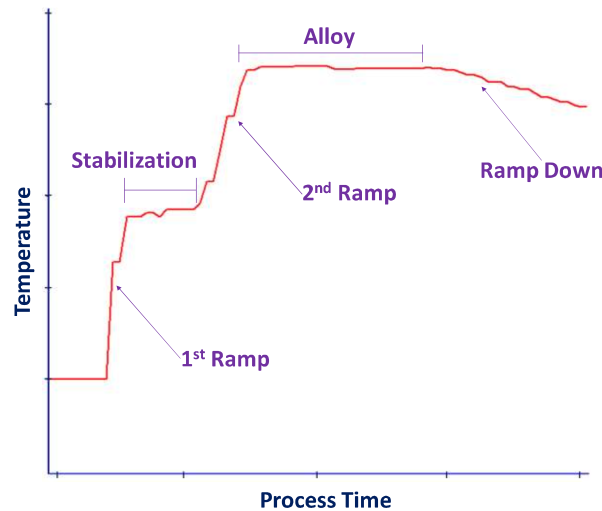

Figure 2. Temperature profile showing heating ramps, intermediate stabilization step, alloying at eutectic temperature, and cool down ramp.

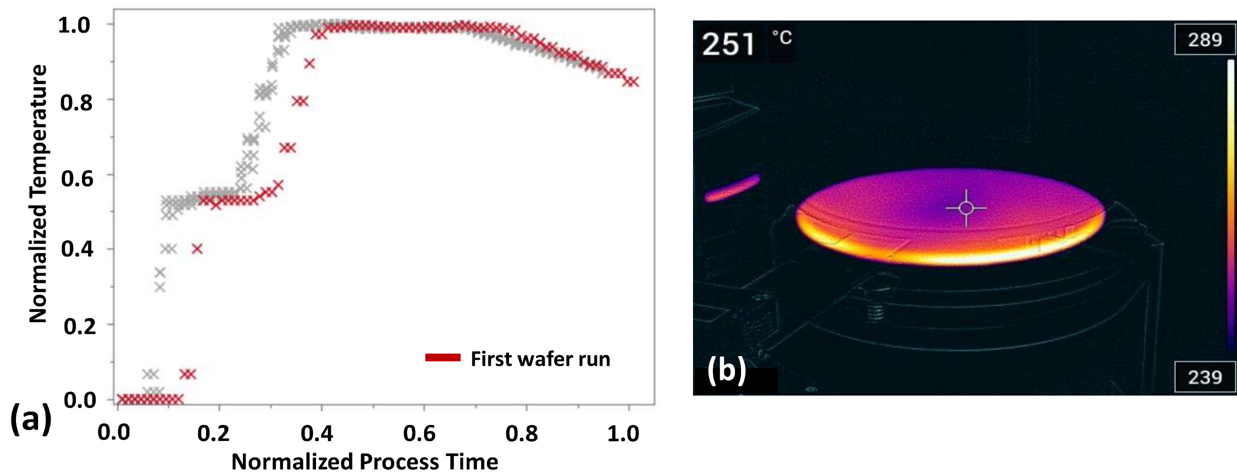

Figure 3. (a) Temperature profile of the first wafer processed through rapid thermal alloying slightly differs from that of the subsequent runs. (b) Temperature distribution map of susceptor with enclosed GaAs product wafer after exiting the quartz furnace for cool down in the ambient environment.

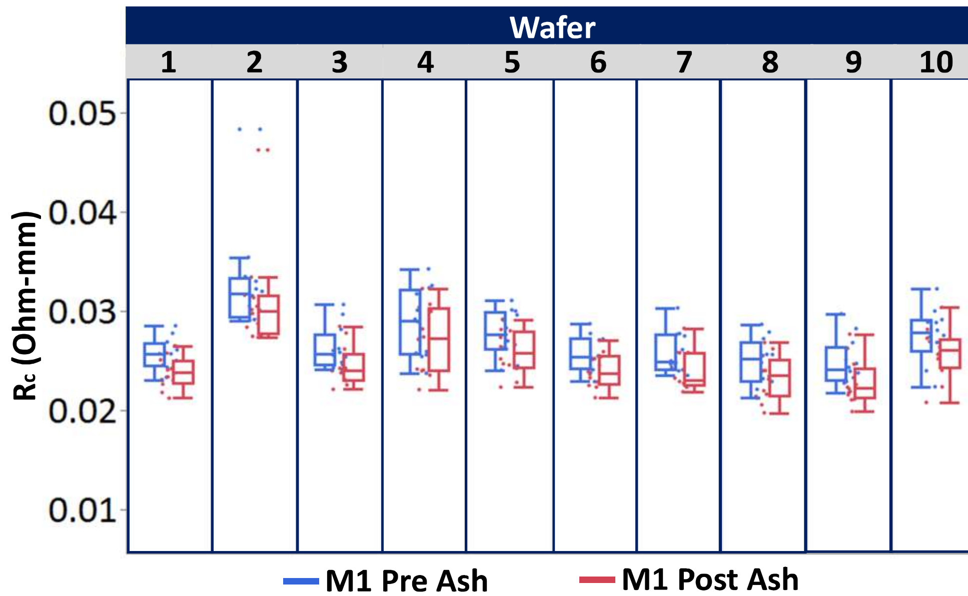

Figure 4. Highly oxidative and thermal ash treatment at M1 stage resulted in a downwards shift in R_c.

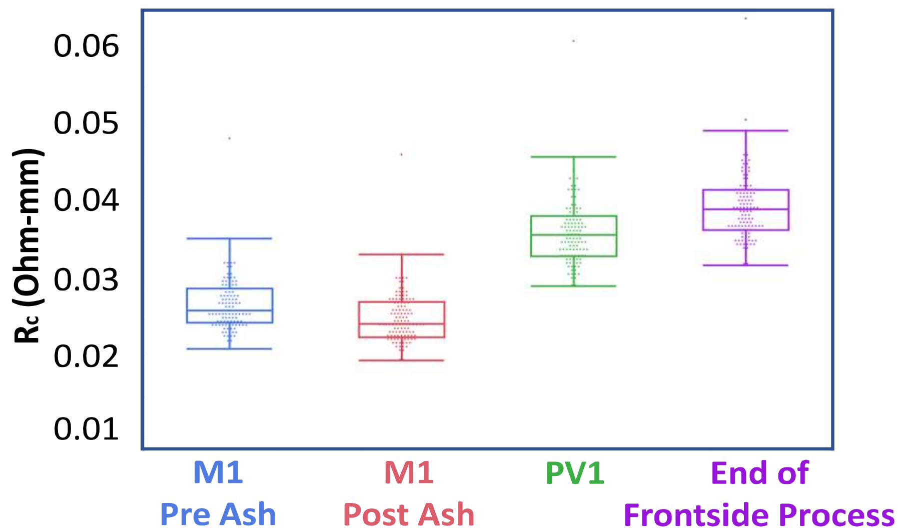

Figure 5. Progression of R_c measured at several stages downstream from the alloy step: M1, PV1, and end of frontside process.

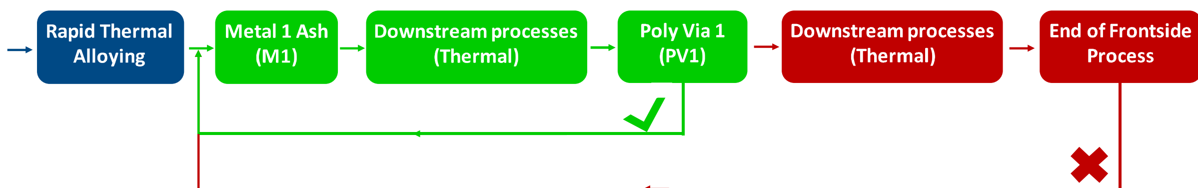

Figure 6. Comparable R_c measured at PV1 and end of frontside process allowed shortened feedback loop for earlier electrical testing of collector-related parameters.