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Choosing the Optimal Internal or External Clocking Solution for FPGA Based Designs

Field programmable gate arrays (FGPAs) are used in a large variety of applications ranging from embedded computing to high-speed serial digital communications. With reconfigurable hardware and dense high-speed logic functions, FPGAs are ideal for implementing high-performance, flexible designs. As part of their high-density architectures, FPGAs contain internal integer and fractional phase-locked loops (PLLs) for frequency synthesis.

This architecture leads to a simple question: To optimize performance and simplify design, when should an FPGA-based design use an internal PLL versus a discrete oscillator or clock IC?

Control Plane Timing

FPGA internal PLLs provide low-skew clock sources for functional blocks including high-speed logic, digital signal processing and embedded memory. Internal PLLs are also used to generate global and regional clocks and other high fan-out, low-skew control signals. External input reference clocks are required to drive these internal PLLs. As shown in Figure 1, simple fixed-frequency oscillators are often used to provide these references. Developers should consider three key criteria when selecting an oscillator to provide FPGA control plane timing:

Long Term Reliability

FPGAs are typically used in applications that have long life cycles, which makes it important to ensure that all board-level components are rated for long-term operation. Oscillators are a key concern since quartz crystal-based components are responsible for the highest rate of field returns in many electronics applications. Crystals are susceptible to contamination issues that can affect start-up and frequency drift over time and temperature.

To ensure long-term reliability, developers should select oscillators that guarantee long-term operation. The appropriate oscillator should guarantee at least a 10-year operating life and specify lifetime aging at an accelerated temperature (e.g., 40 degrees Celsius or higher).

Board Level Noise Immunity

FPGAs typically operate in noisy environments surrounded by switching power supplies. In addition, FPGAs generate noise affecting VDD and ground planes. Minimizing this noise can be relatively expensive and cannot be eliminated completely.

When selecting an oscillator, an important consideration is power supply noise filtering. Oscillators with internal power supply voltage regulation provide noise rejection, enabling more resilient operation by ensuring the device does not violate its stated jitter specifications when subjected to system-level noise.

Availability

Oscillators can take significant time to procure due to the material-intensive, complex manufacturing process associated with quartz processing, die assembly and packaging. Custom frequency oscillators can take even longer to obtain. Choose oscillators that are available for rapid, quick-turn delivery, either in stock at distributors or quickly programmable by the supplier. Fast component availability eases prototyping and enables a speedier design.

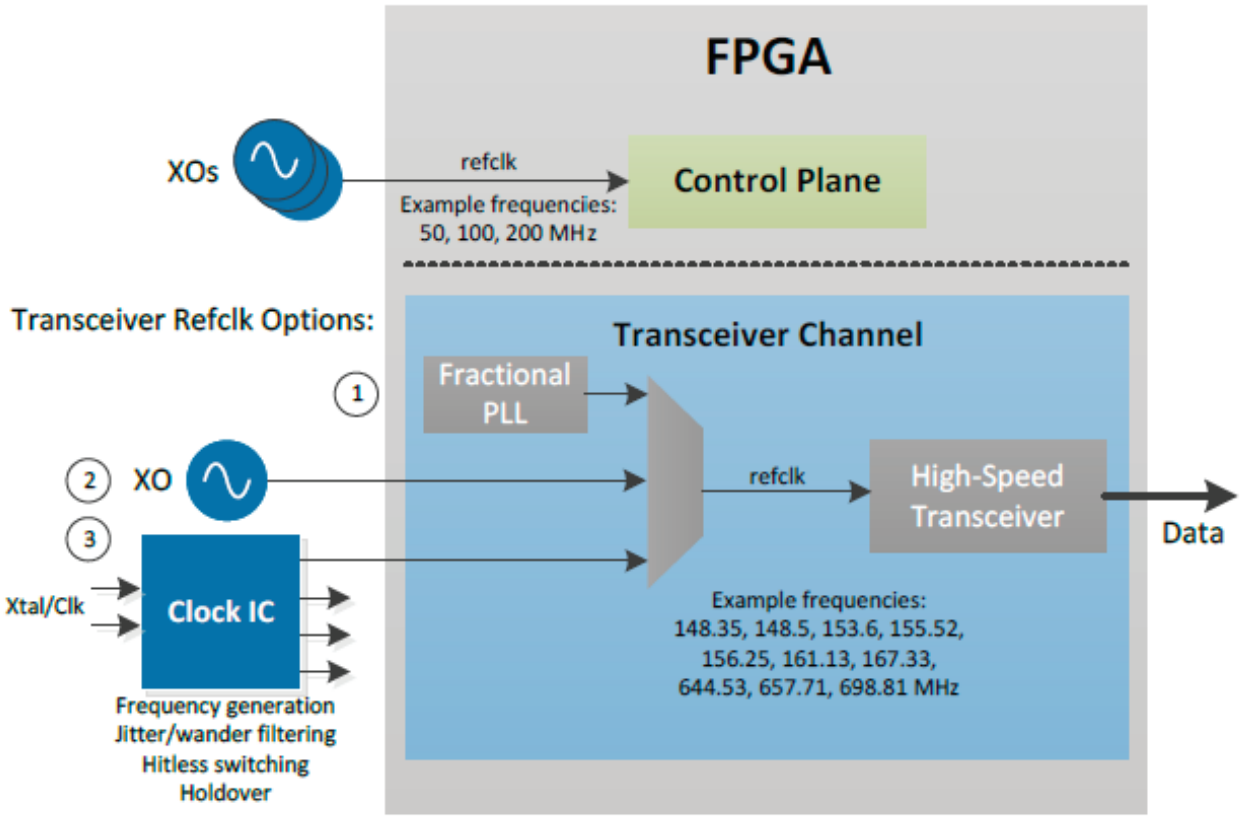


Figure 1. External and Internal Reference Timing Options for FPGAs

Transceiver Clocking

In addition to reliability, power supply noise rejection performance and availability, developers should consider other factors for FPGA-based transceiver clocking applications. For high-speed serial data communications (e.g., 10/40/100G Ethernet, Optical Transport Networking [OTN], 3G-SDI, CPRI and PCI Express), reference clock selection is critical because clock jitter adversely impacts transceiver bit-error rate. Complicating matters, multi-rate applications require a range of different reference frequencies. As shown in Figure 1, hardware designers typically have three transceiver reference clock options:

Internal Integer or Fractional PLL

High performance FPGAs include internal integer/fractional PLLs that can be used for transceiver clocking. These PLLs offer the lowest jitter when operating in integer mode. When used for fractional clock synthesis, some jitter performance is sacrificed.

While the jitter performance of this solution is acceptable for some applications, discrete oscillators and clocks can provide lower jitter and better optimize FPGA transceiver performance.

Oscillator

Single frequency oscillators are available for clocking fixed-rate applications. For multi-rate transceivers, I2C programmable oscillators that are serially programmable to a wide range of frequencies are a superior solution. One benefit of I2C programmable oscillators is they can be used in conjunction with an FPGA's integer PLL.

The oscillator can provide low-jitter fractional clock synthesis, and the FPGA's internal PLL can provide further integer clock multiplication and low skew clock routing.

Clock Generator / Jitter Attenuating Clock IC

The highest performance method for clocking multiple FPGA transceivers is to use a multi-output clock generator/jitter attenuating clock. Frequency-agile clock generators can be used for clocking transceivers in addition to providing control plane clocking. A jitter-attenuating clock IC is required for applications that require synchronization (e.g., SONET/SDH, Synchronous Ethernet, broadcast video and CPRI). These devices integrate ultra-low phase noise voltage-controlled oscillators (VCOs) with a low bandwidth PLL (0.1 Hz to 1 kHz typical) to provide jitter/wander filtering in addition to ultra-low jitter frequency synthesis.

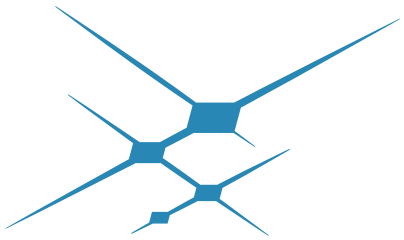
Jitter-attenuating clocks also provide hitless switching, a feature that absorbs the phase difference between two input clocks during a switchover. This minimizes the risk that downstream low-bandwidth PLLs will lose lock due to a clock rearrangement. Finally, jitter-attenuating clocks provide a holdover reference clock function, ensuring transceivers maintain proper operation in the event the reference clock is not available. This mission-critical feature is essential for communications applications that require 99.999% availability.

Conclusion

Ultimately, it is up to the hardware engineer to select the right combination of internal and external clocking solutions for their FPGA-based applications. Now more than ever, hardware designers have a wide range of timing choices (see Table 1) to choose from to optimize their next design.

Device	Description	Output Frequency	Phase Jitter
Si510/11	Single-frequency low-jitter XO	0.1 – 250 MHz	0.8 ps
Si514	I²C-programmable low-jitter XO		
Si530/31	Single-frequency ultra-low-jitter XO	10 – 1417 MHz	0.3 ps
Si570	I²C-programmable low-jitter XO		
Si53306	Universal clock buffer/level translator, 4 outputs	1 – 725 MHz	45 fs
Si53301	Universal clock buffer/level translator, 6 outputs		
Si53302	Universal clock buffer/level translator, 10 outputs		
Si5335	Any-frequency, any-output clock generator, pin control	1 – 350 MHz	1 ps
Si5338	Any-frequency, any-output clock generator, I²C control	0.160 – 710 MHz	
Si5317	Jitter cleaner, pin control	1 – 710 MHz	0.3 ps
Si5326	Any-frequency jitter-attenuating clock, I²C/SPI control	0.002 – 1417 MHz	
Si5328	10/40/100G synchronous Ethernet clock, I²C/SPI	0.008 – 808 MHz	

Table 1. Recommended Skyworks Devices for FPGA-based Applications



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